What is claimed is:

1. A memory device, comprising:

a memory transistor comprising a tunnel insulating layer, first conductive layer patterns, and second conductive layer patterns stacked on a first portion of a semiconductor substrate, and a common source region and a floating junction region arranged at opposite sides of the second conductive layer patterns; and

a selection transistor, which is connected to the floating junction region, the selection transistor comprising a gate insulating layer, the first conductive layer patterns, and the second conductive layer patterns stacked on a second portion of the semiconductor substrate, and a drain region arranged at one side of the second conductive layer patterns opposite the floating junction region,

wherein the first conductive layer patterns in the memory transistor are separated by cell unit and floated, wherein the insulating layer and the second conductive layer patterns stacked on the first conductive layer patterns are connected to a cell and an adjacent cell, and wherein the first conductive layer patterns and the second conductive layer patterns of the selection transistor are etched and connected by metal plugs.

2. The device of claim 1, wherein the first conductive layer patterns and the second conductive layer patterns comprise polysilicon layers to which impurities are doped.

3. The device of claim 1, wherein the metal plugs comprise a tungsten layer.

4. The device of claim 1, wherein the first conductive layer patterns and the second conductive layer patterns of the selection transistor are etched at portions of inactive regions and connected by the metal plugs.

5. A method of fabricating an EEPROM memory device, comprising the steps of:

forming a tunnel insulating layer and a gate insulating layer on a semiconductor substrate on which active regions are defined;

forming a first conductive layer on the semiconductor substrate on which the tunnel insulating layer and the gate insulating layer are formed;

patterning the first conductive layer to form first conductive layer patterns, which are separated by cell unit, in a memory transistor, and first conductive layer patterns, which are broken in a word line direction, in a selection transistor;

forming an insulating layer on the first conductive layer patterns and inactive regions;

forming a second conductive layer on the insulating layer;

patterning the second conductive layer to form second conductive layer patterns having contact holes in the selection transistor;

patterning the second conductive layer patterns to form a sense line of the memory transistor and a word line of the selection transistor;

forming an interlevel insulating layer having metal contact holes exposing the first conductive layer patterns on the semiconductor substrate; and

forming metal plugs in the metal contact holes to connect the first conductive layer patterns, which are broken in the word line direction, and the second conductive layer patterns by the metal plugs.

6. The method of claim 5, further comprising implanting field ions into the inactive regions after the first conductive layer is formed.

7. The method of claim 6, wherein the same masks are used to implant the field ions and form the first conductive layer patterns.

8. The method of claim 5, wherein the metal plugs comprise tungsten.

9. The method of claim 5, wherein the contact holes and the metal contact holes are formed on the inactive regions.

10. A method of fabricating an EEPROM memory device comprising a plurality of memory cells, comprising the steps of:

depositing a first conductive layer on a semiconductor substrate having active and inactive regions, and patterning the first conductive layer to form floating gates and first wordline portions;

depositing an insulating layer;

depositing a second conductive layer and etching the second conductive layer to form first contacts holes in the second conductive layer, and patterning the second conductive layer to form sense line contacts and second wordline portions;

depositing an interlevel insulating layer and forming second contact holes in the interlevel insulating layer corresponding to the first contact holes in the second conductive layer; and

filling the first and second contact holes with a conductive material to connect the first wordline portions of the first conductive layer and the second wordline portions of the second conductive layer to connect adjacent memory cells to a wordline.

11. The method of claim 10, further comprising implanting field ions into the inactive regions after the first conductive layer is formed.

12. The method of claim 11, wherein the same masks are used to implant the field ions and pattern the first conductive layer.

13. The method of claim 10, wherein the conductive material comprises tungsten.

14. The method of claim 10, wherein the first and second contact holes are formed over the inactive regions.